RECEIVED
CENTRAL FAX CENTER

NOV 2 7 2006

REMARKS

I. Introduction

In response to the Office Action dated July 27, 2006, claims 1 and 11 have been amended. Claims 1-20 remain in the application. Re-examination and re-consideration of the application, as amended, is requested.

II. Prior Art Rejections

In paragraph 3, claims 1-2, 4-6, 11-12, 14-16 were rejected under 35 U.S.C. §103(a) as being obvious in view of Wurzer et al, "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz f_T Silicon Bipolar Technology," in view of U.S. Patent No. 5,373,257 (Shimoda). In paragraph 4, claims 3-13 were rejected under 35 U.S.C. 103(a) as being obvious in view of Wurzer in view of Shimoda and further in view of Savoj et al., "A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection." In paragraph 5, claims 7-10 and 17-20 were rejected under 35 U.S.C. 103(a) as being obvious over Wurzer in view of Shimoda and further in view of U.S. Patent No. 6,690,243 (Henrion).

Applicants' claimed invention is patentable over the cited references because it recites elements not taught or suggested by the references. Specifically, the references describe different devices and/or different technologies:

1. Wurzer differs from Applicants' claimed invention in that it describes a Clock and Data Recovery circuit with an input data rate of 40 Gb/s, but a clock rate of 20 Gb/s, which is implemented in silicon bipolar technology, rather than CMOS technology. Moreover, Wurzer does not have a voltage-to-current converter or loop filter, as recited in Applicants' claims.
2. Shimoda differs from Applicants' claimed invention in that it describes a Phase Synchronization circuit, but does not identify the input data rate, clock rate or implementation technology. Moreover, Shimoda is cited by the Office Action only for teaching a loop filter comprising a voltage-to-current converter.
3. Savoj differs from Applicants' claimed invention in that it describes a Clock and Data Recovery circuit with an input data rate of 10 Gb/s, but a clock rate of 5 Gb/s, although the circuit is implemented in CMOS technology. Moreover, Savoj

is cited by the Office Action only for teaching half-quadrature phases of a clock signal that are outputted to a phase detector.

4. Henrion differs from Applicants' claimed invention in that it describes a multi-phase voltage controlled oscillator that outputs four phase offsets of a clock signal with an input data rate of 10 Gb/s and a clock rate of 2.5 Gb/s, and does not describe the use of CMOS technology. Moreover, Henrion is cited by the Office Action only for teaching half-quadrature phases of a clock signal and a ring oscillation structure.

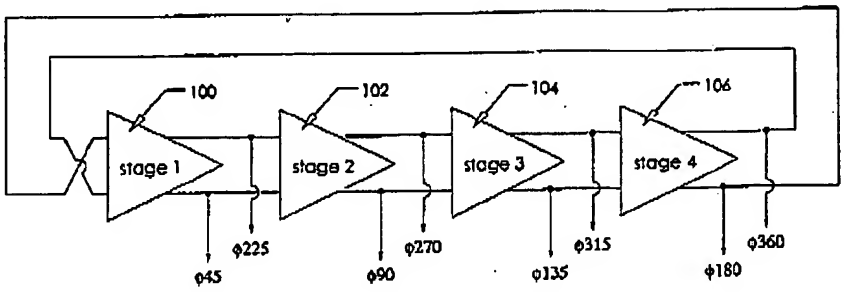
Thus, the references, taken individually or in combination, do not teach or suggest a clock and data recovery circuit or method where the 40 Gb/s input data signal is re-timed and de-multiplexed into four 10 Gb/s output data signals by a phase detector using half-quadrature phase offsets of the 10 Gb/s clock signal, such that each of the 10Gb/s output data signals detects an edge or transition in the 40 Gb/s input data signal and whether the edge or transition is early or late with respect to its corresponding phase of the 10 Gb/s clock signal. Moreover, the references, taken individually or in combination, do not teach or suggest implementing such a circuit in CMOS.

Consequently, Applicants' attorney submits that independent claims 1 and 11 are allowable over Wurzer, Shimoda, Savoj and/or Henrion, because the references, taken individually or in combination, do not teach exactly the same circuit as Applicants' claimed invention. Further, dependent claims 2-10 and 12-20 are submitted to be allowable over Wurzer, Shimoda, Savoj and/or Henrion in the same manner, because they are dependent on independent claims 1 and 11, respectively, and because they contain all the limitations of the independent claims.

With regard to claims 2-6 and 12-16, these claims stand or fall with their respective independent claims 1 and 11. On the other hand, separate arguments for the patentability of claims 7-10 and 17-20 are provided below.

For example, with regard to claims 7 and 17, which recite that the voltage-controlled oscillator is based on differential stimulus of a closed-loop transmission line at equally-spaced points that sustains a phase separation of 180° at diagonally-opposite nodes, providing 45° phase steps in between for the clock signal, the Office Action asserts that these limitations are shown by Henrion at col. 6, lines 47-50.

However, this portion of Henrion merely describes "[a]n eight-phase, four-stage "ring" oscillator is a multi-stage oscillator, wherein a signal experiences a phase shift of 45.degree. at the oscillator frequency as it propagates through each stage," in the context of FIG. 3 thereof:



U.S. Patent Feb. 10, 2004 Sheet 3 of 13 US 6,690,243 B1

Fig. 3

This structure of Henrion does not show a closed-loop transmission line having equally-spaced points that sustains a phase separation of 180° at diagonally-opposite nodes. Consider, for example, the structure of Applicants' VCO 12, as shown in FIG. 2:

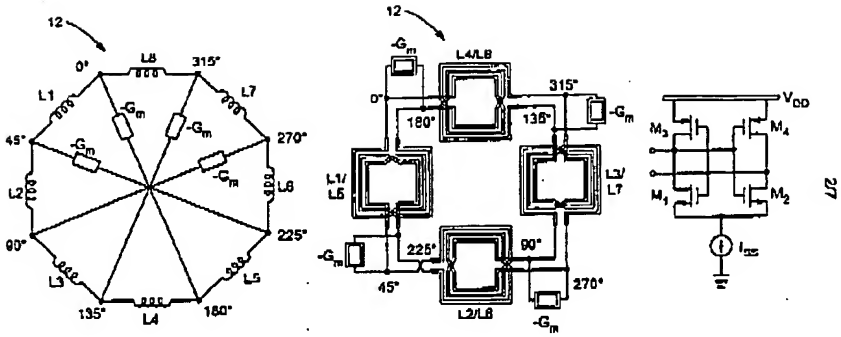


FIG. 2A FIG. 2B FIG. 2C

Consequently, Applicants' attorney submits that dependent claims 7 and 17 are allowable over Wurzer, Shimoda and Henrion, because the references, taken individually or in combination, do not teach exactly the same circuit as Applicants' claimed invention.

Similar arguments apply to claims 8 and 18, which recite that the voltage-controlled oscillator's oscillation frequency is uniquely given by a travel time of a wave around the loop. The same location in Henrion is cited by the Office Action, namely col. 6, lines 47-50, which merely states that the signal experiences a phase shift of 45.degree at the oscillator frequency as it propagates through each stage of an eight-phase, four-stage ring oscillator. However, the oscillator in Henrion is of a different structure than Applicants' claimed oscillator, and the frequency of the oscillator in Henrion is not given by the travel time of a wave around the loop.

With regard to claims 9 and 19, which recite that inductor elements of the voltage-controlled oscillator are grouped into differential structures and $-G_m$ cells are placed in close proximity to the nodes of the voltage-controlled oscillator, the Office Action asserts that these limitations are shown by Henrion in FIG. 7.

However, FIG. 7 of Henrion merely shows the following:

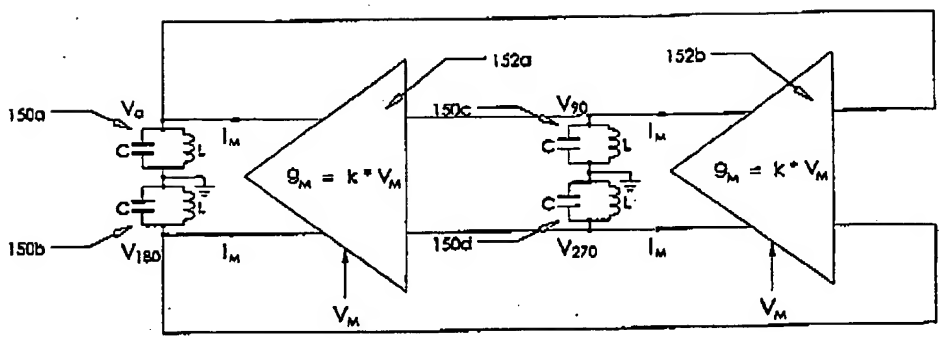


Fig. 7

This figure shows a 4-phase LC oscillator circuit connected in a ring configuration, where the signal is offset by a phase angle of 90 degrees at V0, V90, V180 and V270. The circuit is represented as a two-stage oscillator, each stage consisting of a pair of parallel resonant (tank) LC circuits 150a-b and 150c-d, and an associated transconductance amplifier 152a and 152b

Again, this structure of Henrion does not show the same structure as Applicants' claimed invention, namely a closed-loop transmission line having equally-spaced points that sustains a phase separation of 180° at diagonally-opposite nodes, as shown in the structure of Applicants' VCO 12 in FIG. 2 above.

Consequently, Applicants' attorney submits that dependent claims 9 and 19 are allowable over Wurzer, Shimoda and Henrion, because the references, taken individually or in combination, do not teach exactly the same circuit as Applicants' claimed invention.

Finally, with regard to claims 10 and 20, which recite that each differential port of the voltage-controlled oscillator is buffered by an inductively-loaded differential pair of switches, the Office Action asserts that these limitations are shown by Henrion in FIG. 7. This is

erroneous, because the ports V0, V90, V180 and V270 shown in FIG. 7 of Henrion are not differential ports and are not buffered by an inductively-loaded differential pair of switches. Indeed, nowhere is a similar structure shown in Henrion.

Consequently, Applicants' attorney submits that dependent claims 10 and 20 are allowable over Wurzer, Shimoda and Henrion, because the references, taken individually or in combination, do not teach exactly the same circuit as Applicants' claimed invention.

III. Conclusion

In view of the above, it is submitted that this application is now in good order for allowance and such allowance is respectfully solicited.

Should the Examiner believe minor matters still remain that can be resolved in a telephone interview, the Examiner is urged to call Applicants' undersigned attorney.

Respectfully submitted,

GATES & COOPER LLP
Attorneys for Applicants

Howard Hughes Center
6701 Center Drive West, Suite 1050
Los Angeles, California 90045
(310) 641-8797

By: _____
Name: George H. Gates
Reg. No.: 33,500

Date: November 27, 2006

GHG/

G&C 30435.179-US-U1